Port Map Worksheet: PIC32MX460F512L, MMB32 V1.0

Port A	5VT	HDR1	HDR2	Usage	Description
RA0	Y			*Not connected*	
RA1	Y			*Not connected*	
RA2/SCL2	Y		14		
RA3/SDA2	Y		13		
RA4	Y			*Not connected*	
RA5	Y			*Not connected*	
RA6	Y			SD-CD#	Secure Digital Card Detect (Active Low)
RA7	Y		6		
RA8	-			*No pin*	
RA9/Vref-/Cvref-/PMA7	N			*Not connected*	
RA10/Vref+/Cvref+/PMA6	N			*Not connected*	
RA11 … RA13	-			*No pin*	
RA14/SCL1/INT3	Y			SCL1	Codec I2C connection
RA15/SDA1/INT4	Y			SDA1	Codec I2C connection

Port B	5VT	HDR1	HDR2	Usage	Description
RB0/PGED1/AN0/CN2	N		24		
RB1/PGEC1/AN1/CN3	N		23		
RB2/AN2/C2IN-/CN4	N		22		
RB3/AN3/C2IN+/CN5	N		21		
RB4/AN4/C1IN-/CN6	N			*Not connected*	
RB5/AN5/C1IN+/VBusOn/CN7	N			*Not connected*	
RB6/PGEC2/AN6/OCFA	N			Pgm/Debug	
RB7/PGED2/AN7	N			Pgm/Debug	
RB8/AN8/C1OUT	N		20		
RB9/AN9/C2OUT	N		19		
RB10/AN10/VRefOut/PMA13	N			LCD-YD	Resistive Touch Screen, Y Lower
RB11/AN11/PMA12	N			LCD-XR	Resistive Touch Screen, X Right
RB12/AN12/PMA11	N			LCD-YU	Resistive Touch Screen, Y Upper
RB13/AN13/PMA10	N			LCD-XL	Resistive Touch Screen, X Left
RB14/AN14/PMALH/PMA1	N		18		
RB15/AN15/OCFB/PMALL/PMA0/CN12	N			LCD-RS	LCD Register Select

Port C	5VT	HDR1	HDR2	Usage	Description
RC0	-			*No pin*	
RC1/T2CK	Y			LCD-RST	LCD Reset Line
RC2/T3CK	Y			EE-CS#	Serial Flash Chip Select (Active Low)
RC3/T4CK	Y			*Not connected*	
RC4/T5CK/SDI1	Y			SDI1	Data from the Codec
RC5 … RC11	-			*No pin*	
RC12/OSC1	N			CLKI	8 MHz Crystal
RC13/SOSCI/CN1	N			SOSCI	32,768 Hz Crystal
RC14/SOSCO/T1CK/CN0	N			SOSCO	32,768 Hz Crystal
RC15/OSC2	N			CLKO	8 MHz Crystal

Port D	5VT	HDR1	HDR2	Usage	Description
RD0/SDO1/OC1/INT0	Y			SDO1	Data to the Codec
RD1/OC2	Y		8		
RD2/OC3	Y			LCD-BLED	LCD Backlight LED control. (Open Drain)
RD3/OC4	Y		7		
RD4/OC5/PMWR/CN13	Y	20		PMWR	PM Bus Write Signal (Active Low)
RD5/PMRD/CN14	Y	19		PMRD	PM Bus Read Signal (Active Low)
RD6/PMD14/CN15	Y	17		PMD14	PM Data Bus
RD7/PMD15/CN16	Y	18		PMD15	PM Data Bus
RD8/RTCC/IC1	Y			*Not connected*	
RD9/SS1/IC2	Y			LRC	Codec LRC
RD10/SCK1/IC3/PMCS2/PMA15	Y			SCK1	Codec Clock
RD11/IC4/PMCS1/PMA14	Y		9		
RD12/IC5/PMD12	Y	15		PMD12	PM Data Bus
RD13/PMD13/CN19	Y	16		PMD13	PM Data Bus
RD14/U1CTS/CN20	Y	23			
RD15/U1RTS/CN21	Y	24			

Port E	5VT	HDR1	HDR2	Usage	Description
RE0/PMD0	Y	3		PMD0	PM Data Bus
RE1/PMD1	Y	4		PMD1	PM Data Bus
RE2/PMD2	Y	5		PMD2	PM Data Bus
RE3/PMD3	Y	6		PMD3	PM Data Bus
RE4/PMD4	Y	7		PMD4	PM Data Bus
RE5/PMD5	Y	8		PMD5	PM Data Bus
RE6/PMD6	Y	9		PMD6	PM Data Bus
RE7/PMD7	Y	10		PMD7	PM Data Bus
RE8/INT1	Y			*Not connected*	
RE9/INT2	Y			*Not connected*	

Port F	5VT	HDR1	HDR2	Usage	Description
RF0/PMD11	Y	14		PMD11	PM Data Bus
RF1/PMD10	Y	13		PMD10	PM Data Bus
RF2/U1RX	Y	21			
RF3/USBID	Y			USB-ID	
RF4/U2RX/PMA9/CN17	Y		17		
RF5/U2TX/PMA8/CN18	Y		16		
RF6 … RF7	-			*No pin*	
RF8/U1TX	Y	22			
RF9 … RF11	-			*No pin*	
RF12/U2CTS	Y			LCD-CS#	LCD Chip Select Line (Active Low)
RF13/U2RTS	Y		15		

Port G	5VT	HDR1	HDR2	Usage	Description
RG0/PMD8	Y	11		PMD8	PM Data Bus
RG1/PMD9	Y	12		PMD9	PM Data Bus
RG2/D+	N			D+	USB Data Bus
RG3/D-	N			D-	USB Data Bus
RG4 … RG5	-			*No pin*	
RG6/SCK2/PMA5/CN8	Y		10	SCK2	SPI2 Clock
RG7/SDI2/PMA4/CN9	Y		11	SDI2	SPI2 MISO
RG8/SDO2/PMA3/CN10	Y		12	SDO2	SPI2 MOSI
RG9/SS2/PMA2/CN11	Y			SD-CS#	Secure Digital Card Select (Active Low)
RG10 … RG11	-			*No pin*	
RG12	Y		4		
RG13	Y		3		
RG14	Y		5		
RG15	Y			*Not connected*	

Other	5VT	HDR1	HDR2	Usage	Description
Vcc 3.3v	-	1,25	25	Vcc 3.3v	Power from internal regulator
Vcc 5.0v	-		1	Vcc 5.0v	External power or Vbus from USB
Vss	-	2,26	2,26	Vss	Ground
MCLR# on CN1 pin 4 & CN9 pin 6	Y			MCLR	The PIC32 reset line (Active Low)

Legend

Pin available or sharable
Pin used internally
Pin invalid or unavailable

5VT: Y means this pin can tolerate up to 5V in input mode. N means the input must never exceed Vdd.
HDR1 and HDR2 refer to the two 26-pin single-in-line header connections.
CN1 and CN9 refer to the debug/programming ports.

Notes:

References to the JTAG and TRACE interfaces are omitted.
The Secure Digital Card and Serial Flash chip both utilize SPI port 2. This port is available for expansion.

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