PIC32MZ Embedded Connectivity (EC) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity (EC) family devices that you have received conform functionally to the current Device Data Sheet (DS60001191**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity (EC) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections (if applicable) start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Embedded Connectivity (EC) family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A3	A4	A5
PIC32MZ1024ECG064	0x05103053	0x3	0x4	0x5
PIC32MZ1024ECH064	0x05108053			
PIC32MZ1024ECM064	0x05130053			
PIC32MZ2048ECG064	0x05104053			
PIC32MZ2048ECH064	0x05109053			
PIC32MZ2048ECM064	0x05131053			
PIC32MZ1024ECG100	0x0510D053			
PIC32MZ1024ECH100	0x05112053			
PIC32MZ1024ECM100	0x0513A053			
PIC32MZ2048ECG100	0x0510E053			
PIC32MZ2048ECH100	0x05113053			
PIC32MZ2048ECM100	0x0513B053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**C**) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A3	A4	A5
PIC32MZ1024ECG124	0x05117053	0x3	0x4	0x5
PIC32MZ1024ECH124	0x0511C053			
PIC32MZ1024ECM124	0x05144053			
PIC32MZ2048ECG124	0x05118053			
PIC32MZ2048ECH124	0x0511D053			
PIC32MZ2048ECM124	0x05145053			
PIC32MZ1024ECG144	0x05121053			
PIC32MZ1024ECH144	0x05126053			
PIC32MZ1024ECM144	0x0514E053			
PIC32MZ2048ECG144	0x05122053			
PIC32MZ2048ECH144	0x05127053			
PIC32MZ2048ECM144	0x0514F053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001191**C**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
ADC	INT0 Trigger	1.	When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.	X	X	X
ADC	Data Format	2.	Two's complement (signed) input mode does not produce expected results.	X	X	X
Boot Flash	Boot Sequence	3.	When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.	X	X	X
Comparator Voltage Reference	Range Selection	4.	The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function.	X	X	X
Ethernet Controller	Alternate MII and RMII Configurations	5.	The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.	X	X	X
Ethernet Controller	MII Configuration	6.	MII mode is not available on 64-pin devices.	X	X	X
Ethernet Controller	RMII Mode	7.	MII pins that are not used by the Ethernet module during RMII operation may not be available for other functions.	X	X	X
I/O Port	Open Drain	8.	The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.	X	X	X
Oscillator	FRC Tuning	9.	Changing values in the OSCTUN register has no effect on the FRC accuracy.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
Oscillator	Ceramic Resonator	10.	The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).	X	X	X
Secondary Oscillator	Crystal Oscillator	11.	A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).	X	X	X
Reserved	—	12	—	—	—	—
Power-Saving Modes	Dream Mode	13.	Dream mode does not function.	X	X	X
Power-Saving Modes	Sleep Mode	14.	The device may not exit Sleep mode.	X	X	X
SPI	Maximum Speed Operation	15.	The SPI clock speed does not meet the published specification.	X	X	X
Reserved	—	16.	—	—	—	—
System Bus	Permission Access	17.	When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.	X	X	X
USB	Suspend Mode	18.	The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.	X	X	X
USB	—	19.	The USB module requires a start-up delay.	X	X	X
USB	Endpoint FIFO	20.	Endpoint FIFOs cannot be read using 32-bit reads.	X	X	X
Reserved	—	21.	—	—	—	—
Watchdog Timer	Window Mode	22.	When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.	X	X	X
Watchdog Timer	Reset Trigger	23.	When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a non-maskable interrupt (NMI).	X	X	X
PMP	Address Lines	24.	PMP address lines block the use of lower-order functions when the PMP is used but the corresponding bit in the PMAEN register is cleared.	X	X	X
I2C	Master Stop	25.	Setting the PEN bit to send a Stop does not release the SDA line.	X	X	X
Crypto Engine	Byte Ordering	26.	The Crypto Engine processes data in big-endian order rather than little-endian.	X	X	X
Random Number Generator	True Random Number Generator (TRNG) Mode	27.	TRNG mode does not function.	X	X	X
Flash	Code-Protect	28.	Once the Code-Protect feature is enabled, a device cannot be erased using ICSP or JTAG.	X		
ADC	Group Interrupt	29.	When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register.	X	X	X
SQI	Soft Reset	30.	A Soft Reset is only possible when clock divider values are '0' and '1'.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
SQI	XIP Mode	31.	XIP mode is not operational.	X	X	X
SQI	Buffer Thresholds	32.	Transmit and receive operation may not function properly.	X	X	X
SQI	Interrupts	33.	Some Interrupt Signal Enable bits are set upon a Reset.	X	X	X
SQI	Read Clock Speed	34.	Clock for read operations does not meet the published specification.	X	X	X
SQI	Transmit Buffer Empty Status	35.	Upon a reset, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.	X	X	X
Comparator	Idle Mode	36.	The Comparator cannot be disabled when the device is in Idle mode.	X	X	X
Comparator	Offset	37.	The Comparator offset does not meet the published specification	X	X	X
I/O Pins	SOSCO Function	38.	I/O pins shared with the SOSCO function cannot be used as general purpose input or output.	X	X	X
I2C	Overrun Interrupt	39.	A Slave interrupt is not generated during an overrun condition.	X	X	X
Flash Memory	Program Write Protect	40.	The Program Write Protect (PWP) bits protect all Program Memory.	X	X	X
Oscillator	POSC	41.	A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins).	X	X	
5V Tolerant I/O Pins	Pull-ups	42.	Internal pull-up resistors may not guarantee a logical '1' on digital inputs on 5V tolerant pins.	X	X	X
ADC	—	43.	Dedicated Sample and Hold circuits as well as Automatic Channel scan mode are not supported.	X	X	X
ADC	—	44.	ADC module does not meet published specifications.	X	X	X
Prefetch	Module Disable	45.	Disabling the Prefetch does not invalidate contents.	X	X	X
Oscillator	Clock Switch	46.	Switching the System Clock (SYSCLK) to the Secondary PLL (SPLL) causes a device Reset. This affects both software and hardware (IESO) clock switching.	X	X	X
DMA	Interrupt Trigger	47.	A UART6 Transfer Done interrupt cannot be used to trigger DMA activity.	X	X	X
UART	Auto-baud	48.	The Automatic Baud Rate feature does not function to set the baud rate.	X	X	X
Deadman Timer	NMI	49.	The Deadman Timer triggers a device Reset instead of a Non-Maskable Interrupt (NMI).	X	X	X
Oscillator	POSC Crystal	50.	Crystal support for the Primary Oscillator does not meet published specifications for frequency and voltage.	X	X	X
Reserved	—	51.	—	—	—	—

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: ADC

When using INT0 as a trigger source for ADC conversion, the INT0EP bit in the INTCON register controls which edge triggers the conversion (rising or falling). However, only a rising edge will trigger the conversion.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

2. Module: ADC

Two's complement (signed) input mode does not produce expected results. Signed mode selections are SHxMOD<1:0> = 01 for single-ended or SHxMOD<1:0> = 11 for differential inputs.

Work arounds

Work around 1:

Use two's complement format for all inputs. The Two's complement format works properly when all sample and holds are set for this format. Single ended or differential mode can still be selected independently. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 01, for signed single ended
  or,
- SHxMOD<1:0> = 11, for signed differential inputs

Work around 2:

Use unipolar (unsigned) mode selections for all sample and holds. Where needed, convert the unsigned results to signed values. Unsigned 12-bit results can be converted to signed values by subtracting 2048 from the signed result. Use one of the following settings for SH0MOD through SH5MOD:

- SHxMOD<1:0> = 00, for unsigned single ended
  or,
- SHxMOD<1:0> = 10, for unsigned differential inputs

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

3. Module: Boot Flash

When Boot Flash 1 is selected to be mapped to a Lower Boot Alias memory, the device may instead incorrectly map Boot Flash 2.

Work around

Program an invalid sequence number (such as 0xFFFFFFFF or 0x00000000) into Boot Flash 2. This will force the device to map Boot Flash 1 into the Lower Boot Alias memory.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

4. Module: Comparator Voltage Reference

The Comparator Voltage Reference (CV_{REF}) module range selection (CVRR bit in the CVRCON register) does not function. The default setting of the CV_{REF} Range Selection bit (CVRR) is set to 0 to 0.67 CV_{RSRC}, with a step size of $CV_{RSRC}/24$, and cannot be changed.

Work around

Use an External Voltage Reference and adjust it appropriately to achieve the desired CV_{REF} output.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

5. Module: Ethernet Controller

The Alternate Ethernet pins, AERXDV and AERXCLK, are not available on 100-pin devices.

Work around

Only use either the MII or RMII configuration.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

6. Module: Ethernet Controller

MII mode is not available on 64-pin devices. In this mode, the Ethernet pin, ERXD2, is not available.

Work around

Use the RMII or Alternate RMII configurations.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

7. Module: Ethernet Controller

MII pins that are not used by the Ethernet module during RMII operation are not released, and therefore, lower priority functions on these pins are not available in this mode. However, higher priority functions on these pins, such as EBI and analog inputs (for ADC and Comparators), can still be used.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

8. Module: I/O Port

The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

9. Module: Oscillator

Changing values in the OSCTUN register has no effect on the FRC accuracy.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

10. Module: Oscillator

The Ceramic Resonator cannot be used as an input to the Oscillator module (OSC1/OSC2 pins).

Work around

Instead, use either a crystal oscillator or the external clock.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

11. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).

Work around

Instead, use the external clock.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

12. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

13. Module: Power-Saving Modes

Dream mode is intended as a feature allowing DMA operation while the CPU is in Idle mode; however, Dream mode does not function.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

14. Module: Power-Saving Modes

The device may not exit Sleep mode.

Work arounds

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 configuration register.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

15. Module: SPI

The SPI clock speed does not meet the published specification. The maximum supported SPI clock speed is 27 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

16. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

17. Module: System Bus

When Permission Access is enabled, any access by an initiator that is not allowed will not succeed; however, the status registers may not accurately report the violations.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

18. Module: USB

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

Work around

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

19. Module: USB

The USB module requires a start-up delay.

Work around

When enabling the USB PLL, add a three second delay before turning on the USB module.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

20. Module: USB

Endpoint FIFOs cannot be read using 32-bit reads.

Work around

Use 8-bit reads, reading each portion and copying into a 32-bit value.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

21. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

22. Module: Watchdog Timer

When the Watchdog Timer is used in Window mode, the module may issue a Reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

23. Module: Watchdog Timer

When the Watchdog Timer expires during Sleep mode, it causes a Reset rather than a Non-maskable Interrupt (NMI).

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

24. Module: PMP

PMP address lines block the use of lower-order functions when the PMP is used but the corresponding bit in the PMAEN register is cleared.

For example, on 100-pin devices, pin 2 is EBIA5/ AN34/PMA5/RA5; however, clearing bit 5 of the PMAEN register does not allow RA5 to function as GPIO even though PMA5 is not to be used with the PMP.

Work around

Higher-order functions are available and should be used instead. As described in the previous example, EBIA5 and AN34 would be available.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

25. Module: I^2C

Setting the PEN bit to send a Stop does not release the SDA line.

Work around

The I^2C module must be turned ON before every transaction, and turned OFF after the transaction completes.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

26. Module: Crypto Engine

The Crypto Engine processes data in big-endian order rather than little-endian.

Work around

Use the SWAPEN bit (CECON<5>) to byte-reverse the data on input. After the data is processed, it must be byte-reversed by software or programmable DMA.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

27. Module: Random Number Generator

True RNG mode does not function.

Work around

Instead, use Pseudo-Random Number Generator (PRNG) mode.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

28. Module: Flash

Under normal conditions, once the Code-Protect feature is enabled, a device cannot be accessed (read and/or write) through external interfaces such as ICSP or JTAG. To gain access through these interfaces, the Code-Protect bit must be erased, either by issuing an erase command (using ICSP or JTAG) or with the help of RTSP code. However, the device erase command using ICSP or JTAG does not function, once the Code-Protect feature is enabled.

Work arounds

Work around 1:

Use the RTSP method to update code in a Code-Protect enabled device. In this mode, Flash memory can be erased and programmed with desired data.

Work around 2:

Use the RTSP method with the Live-Update feature of the device to erase the Code-Protect bit. Using this method, the application will erase the Code-Protect bit located in the inactive Boot Flash memory, and update this Boot Flash sequence to a higher number versus the active Boot Flash memory. On the next POR, Boot Flash memory with the erased Code-Protect bit will be used to configure the device, including Code-Protect configuration.

Affected Silicon Revisions

A3	A4	A5					
X							

29. Module: ADC

When using Channel Scan, Class 3 inputs are always part of the Group Interrupt regardless of the setting of the AGIENx bits in the AD1IRQENx register. Conversions should only be part of the Group interrupt if a AGIENx bit is set.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

30. Module: SQI

A SQI Soft Reset, which is controlled by the RESET bit in the SQI1CFG register does work when the CLKDIV<7:0> bits in the SQI1CLKCON register have a value of two or higher.

Work around

Set the CLKDIV<7:0> bits to a value of zero or one.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

31. Module: SQI

XIP mode is not operational (MODE<2:0> bits = `011` in the SQI1CFG register).

Work around

Use PIO mode (MODE<2:0> bits = `001`) or DMA mode (MODE<2:0> bits = `010`).

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

32. Module: SQI

Transmit and receive operation may not function properly.

Work around

Set the TXCMDTHR<5:0> and RXCMDTHR<5:0> bits in the SQI1CMDTHR register to multiples of 4 (32-bit aligned data buffers).

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

33. Module: SQI

The TXEMPTYISE, TXTHRISE, RXEMPTYISE, RXTHRISE, and CONEMPTYISE Interrupt Signal Enable bits in the SQI1INTSEN register are enabled on a device Reset.

Work around

Clear these bits by software.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

34. Module: SQI

Clock speed for read operations does not meet the maximum specification (SQ10) of 50 MHz. For read operations the maximum clock is 25 MHz.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

35. Module: SQI

For all resets, the Transmit Buffer Empty Status (TXEMPTYIF) bit in the SQI1INTSTAT register is cleared to zero instead of being set to one.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

36. Module: Comparator

The SIDL bit in the CMSTAT register is intended to stop all Comparator modules when the CPU enters Idle mode. However, this bit does not function, and all enabled modules will continue to operate.

Work around

Disable the Comparator module by clearing the ON bit in the CMxCON register prior to entering Idle mode

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

37. Module: Comparator

The Input Offset Voltage parameter (D300) is not within the published data sheet specification. The typical value is ±30 mV.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

38. Module: I/O Pins

When the Secondary Oscillator is disabled through the FSOSCEN bit (DEVCFG1<6>), the SOSCO pin does not tri-state and is driven to Vss. An I/O pin shared with the SOSCO function cannot be used as a general purpose input or output.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

39. Module: I^2C

When operating in Slave mode, the I^2C module does not trigger an interrupt when an overrun condition occurs.

Work around

Monitor the I2COV bit in the I2CxSTAT register using software.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

40. Module: Flash Memory

Under normal conditions, setting the Program Write Protect (PWP) bits sets a mark below which the program memory is protected. Memory above this setting may be erased or written. However, the device protects all of program memory when any PWP bits are set.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

41. Module: Oscillator

Depending on the revision of silicon, a crystal oscillator cannot be used as the input to the Primary Oscillator (OSC1/OSC2 pins).

Work around

For Revision A3 and A4 silicon:

Use an external clock or an internal FRC.

For Revision A5 silicon:

See Data Sheet Clarification 3: Primary Oscillator.

Affected Silicon Revisions

A3	A4	A5					
X	X						

42. Module: 5V Tolerant I/O Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load doesn't exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

43. Module: ADC

Note: A related code example is available in the latest release of MPLAB Harmony. For more information, visit http://www.micochip.com/harmony.

The ADC module has the following restrictions:

1. SH0 through SH4 functionality is not supported. Sampling must be performed on SH5 only.
2. Automatic Channel Scan mode is not supported. Channel Scan must be performed manually in software.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

44. Module: ADC

Note: A related code example is available in the latest release of MPLAB Harmony. For more information, visit http://www.micochip.com/harmony.

For Revision A3 and A4 silicon:

The ADC module does not meet the published Throughput Rate (AD51) and Full-Scale Input Range (AD12) specifications. The updated Maximum Throughput Rate (AD51) specification is 125 ksps, assuming 16x Oversampling mode. The updated Maximum Full-Scale Input Range is 2.5V for both Differential and Singled-Ended modes. The updated Minimum Full-Scale Input Range is -2.5V for Differential mode.

For Revision A5 and newer silicon:

The ADC module does not meet published throughput rate (AD51) and accuracy specifications. More information will be provided in a subsequent October 2014 update of this document.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

45. Module: Prefetch

The Prefetch module does not invalidate buffer contents when the module is disabled by setting the PREFEN<1:0> bits to `'b00`.

Work around

To disable the Prefetch module, execute four 32-bit `NOP` commands before and after setting the PREFEN<1:0> bits to `'b00`.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

46. Module: Oscillator

Switching the System Clock (SYSCLK) to the System PLL (SPLL) causes a device Reset. This affects both software and hardware (IESO) clock switching.

Work around

To switch the clock source, disable IESO, and execute the following steps in software:

1. Reduce the speed of all peripheral buses to 128:1 through PBCLKx (where 'x' ≠ 7) and reduce the speed of the CPU bus to 128:1 through PBCLK7.
2. Perform the clock switch.
3. Set the speed of the CPU bus to the previous clock switch divisor and set the speed of the peripheral buses to their previous clock switch divisor.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

47. Module: DMA

The UART6 Transfer Done Interrupt (190) cannot be used to trigger a DMA activity, such as a start or a stop.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

48. Module: UART

The UART Automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

49. Module: Deadman Timer

The Deadman Timer should trigger a Non-Maskable Interrupt (NMI) when the timer runs out or when an incorrect value is written to the DMTPRECLR or DMTCLR registers. Instead, the Deadman Timer triggers a device Reset without a NMI.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

50. Module: Oscillator

The Primary Oscillator does not meet the published specifications for crystal support.

Work around

To use a crystal with the Primary Oscillator, the following limitations on voltage and frequency must be observed:

- 2.4V ≤ V_{DD} ≤ 3.6V
- 4 MHz ≤ Crystal Speed ≤ 24 MHz

Additional details can be found in Data Sheet Clarification 3: Primary Oscillator.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

51. Module: Reserved

The issue previously reported in a prior revision of this errata, is no longer relevant and was removed.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001191**C**):

Note:	Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ADC Configuration Requirements

Note:	A related code example is available in the latest release of MPLAB Harmony. For more information, visit: http://www.micochip.com/harmony.

To meet ADC specifications, the following steps must be performed:

1. Set the ADC Configuration words, as follows:

```
AD1CAL1 = 0xF8894530;
AD1CAL2 = 0x01E4AF69;
AD1CAL3 = 0x0FBBBBB8;
AD1CAL4 = 0x000004AC;
AD1CAL5 = 0x02000002;
```

2. Perform self-calibration. The input mode for SH0-SH5 must be set to the unipolar differential input mode by setting the SHxMOD<1:0> bits (AD1MOD<1:0>) = `10`.

Note:	SH0 through SH4 functionality is not supported, but is required for auto-calibration. Sampling must be performed on SH5 only.

3. ADC module access directly by the CPU of any Special Function Registers while the module is operating is not supported. The ADC must be configured in DMA mode to read result registers.
4. The ADC Clock (i.e.,TAD) must be limited to 1 MHz ≤ TAD ≤ 16 MHz (i.e., 1000 ns ≤ TAD ≤ 62.5 ns.
5. ADC maximum conversion rate:
   a) 125 ksps.
   b) For ADC SH5: SR = ((SAMC + 1)TAD + 4TAD), SAMC(min) = 3.
6. ADC ≥ 16x hardware oversampling is required.

Note:	16x hardware oversampling gives a 14-bit ADC result, 256x hardware oversampling gives a 16-bit ADC result.

7. The first (16) conversion in 16x Oversampling mode after enabling the ADC, regardless of the ADC hardware oversampling filter selected, must be discarded.
8. Use of external low noise voltage reference sources is required (set VREFSEL<2:0> (AD1CON3<12:10>) = `'b011`), with a dedicated external voltage source connected to VREF+, and with VREF- tied to external AVSS.

2. Module: I/O Ports

The injection current for certain I/O pins is higher than specified in the data sheet. The injection current for the pins in **bold** type are listed in the following table.

TABLE 37-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
DI50	IIL	Input Leakage Current (Note 3)					
		I/O Ports (with the following three exceptions)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		SOSCI/RPC13/RC13	**—**	**—**	**±500**	**µA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**
		SOSCO/RPC14/TI1CK/RC14	**—**	**—**	**±500**	**µA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**
		RPF3/USBID/RF3	**—**	**—**	**±500**	**µA**	**VSS ≤ VPIN ≤ VDD, Pin at high-impedance**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

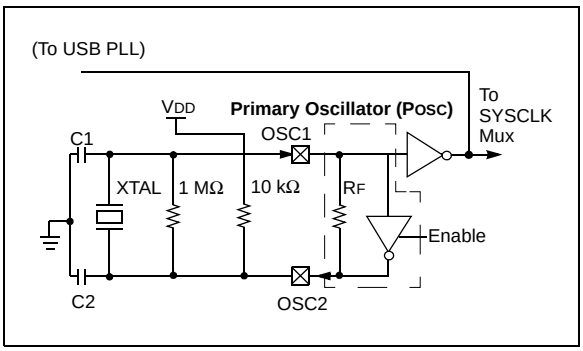
3: Negative current is defined as current sourced by the pin.

3. Module: Primary Oscillator

The Primary Oscillator logic in **Figure 8-1: "PIC32MZ EC Family Oscillator Block Diagram"** of the current device data sheet omitted a pull-up resistor (R_K), which is necessary to ensure stable start-up of the Primary Oscillator when it is running from a crystal. This resistor must be 10 kΩ and connected between OSC2 and V_{DD}.

The following figure shows the amended portion of the diagram.

FIGURE 8-1: PIC32MZ EC FAMILY OSCILLATOR BLOCK DIAGRAM



Crystals with a speed of 4 MHz to 24 MHz that meet the following requirements will meet the PIC32MZ oscillation requirements when configured as depicted in Figure 8-1.

1. Manufacturer Drive Level (min) < 10 µW (hard requirements, 1 µW preferred).
2. Manufacturer ESR ≤ 50Ω (hard requirement, lower is better).

How to Calculate XTAL Capacitive loading:

1. PIC32 C_{IN} = C_{OUT} = ~4 pF (PIC32 OSCI and OSCO package pin capacitance).
2. $C1_{MFG}$ = $C2_{MFG}$ = Manufacturer Recommended Load Capacitance.
3. C_{LOAD} = {([C_{IN} + $C1_{MFG}$] [$C2_{MFG}$ + C_{OUT}]) / [C_{IN} + $C1_{MFG}$ + $C2_{MFG}$ + C_{OUT}]} + estimated PCB stray capacitance (2.5 pF)

   (Simplified) C_{LOAD} = ((C_{IN} + $C1_{MFG}$) / 2) + 2.5 pF).

Actual C1, C2 Load value to use:

- C2 = C_{LOAD}
- C1 = (C_{LOAD} - 2 pF)

Validated Crystals

Temperature Range: (-20ºC to +70ºC)

V_{DD} = 2.4V to 3.6V, R_P = 1 MOhm, R_K = 10 kOhm

- TXC 9B-8.000MAAJ-B, (8 Hz throughhole)
- TXC 9B-12.000MEEJ-B, (12 MHz throughhole)
- TXC 7M-12.000MAAE-T, (12 MHz surface mount)

Temperature Range: (-45ºC to +110ºC)

V_{DD} = 2.4V to 3.6V, R_P = 1 MOhm, R_K = 10 kOhm

- ABLS-12.000MHz-L4Q-T, (12 MHz surface mount)

4. Module: Internal FRC Oscillator

Certain specifications were stated incorrectly in the data sheet. The correct values are shown in **bold** type in the following table.

TABLE 37-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	**-5**	**+/-0.9**	**+5**	**%**	**-40°C ≤ TA ≤ +105°C**

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

APPENDIX A: REVISION HISTORY

Rev A Document (11/2013)

Initial release of this document, issued for revision A3 silicon.

This version includes the following issues: 1 (ADC), 2 (ADC), 3 (Boot Flash), 4 (Comparator Voltage Reference), 5 (Ethernet Controller), 6 (Ethernet Controller), 7 (Ethernet Controller), 8 (I/O Port), 9 (Oscillator), 10 (Oscillator), 11 (Secondary Oscillator), 12 (LPRC Oscillator), 13 (Power-Saving Modes), 14 (Power-Saving Modes), 15 (SPI), 16 (SQI), 17 (System Bus), 18 (USB), 19 (USB), 20 (USB), 21 (USB), 22 (Watchdog Timer), 23 (Watchdog Timer), 24 (PMP), 25 (I2C), 26 (Crypto Engine), and 27 (Random Number Generator).

Rev B Document (12/2013)

Updated issues 7 (Ethernet Controller) and 14 (Power-Saving Modes).

Content in issue 21, which was included in a previous errata version, was removed and this issue has been marked as **Reserved**.

Added data sheet clarification issues 1 (Power-Down Current) and 2 (Operating Conditions), and silicon issues 28 (Flash) and 29 (ADC).

Rev C Document (4/2014)

Updated for revision A4 silicon.

Content in issues 12 and 16, which was included in a previous errata version, was removed and these issues have been marked as **Reserved**.

Added silicon issues 30 (SQI), 31 (SQI), 32 (SQI), 33 (SQI), 34 (SQI), 35 (SQI), 36 (Comparator), 37 (Comparator), 38 (I/O Pins), 39 (I2C), 40 (Flash Memory), 41 (Oscillator), 42 (5V Tolerant I/O Pins), 43 (ADC), 44 (ADC), and 45 (Prefetch).

Added data sheet clarification issues 3 (Internal FRC Accuracy), 4 (Internal LPRC Accuracy), 5 (Internal Backup FRC (BFRC) Accuracy), 6 (ADC1 Module Specifications and Timing Requirements), 7 (ADC Configuration Requirements), 8 (SQI Timing Requirements), 9 (DC Temperature and Voltage Specifications.), 10 (Recommended Minimum Connection), and 11 (I/O Ports).

Rev D Document (5/2014)

Updated silicon issues 43 (ADC) and 44 (ADC) and data sheet clarifications 6 (ADC1 Module Specifications and Timing Requirements) and 7 (ADC Configuration Requirements).

Rev E Document (9/2014)

Updated for revision A5 silicon.

Updated silicon issues 24 (PMP), 25 (I2C), and 41 (Oscillator).

Added silicon issues 46 (Oscillator), 47 (DMA), 48 (UART), 49 (Deadman Timer), 50 (Oscillator), and 51 (Reserved).

Removed data sheet clarifications 1 through 6 and 8 through 11. Issue 7 was retained, which is now issue 1 (ADC Configuration Requirements).

Added data sheet clarifications 2 (I/O Ports) and 3 (Primary Oscillator).

Rev F Document (10/2014)

Content in issue 51, which was included in the previous errata version, was removed and this issue have been marked as **Reserved**.

Updated issue 44 (ADC).

Added data sheet clarification 4 (Internal FRC Oscillator).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-63276-695-3

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Pforzheim
Tel: 49-7231-424750

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

03/25/14